

Fig.1

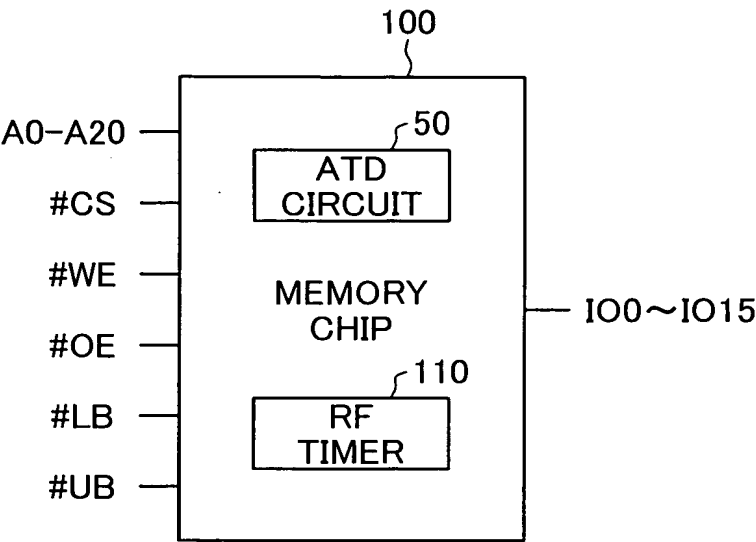


Fig.2

	#CS	REFRESH MODE (*)
OPERATION	L	MODE 1
STANDBY	H	MODE 2

- (*)
- REFRESH MODE 1 : REFRESH OPERATION IS EXECUTED SYNCHRONOUSLY WITH PATD SIGNAL AFTER REFRESH TIMING SIGNAL IS GENERATED IN MEMORY CHIP
- REFRESH MODE 2 : REFRESH OPERATION IS EXECUTED IN RESPONSE TO GENERATION OF REFRESH TIMING SIGNAL IN MEMORY CHIP (ADDRESS INPUT UNNECESSARY)

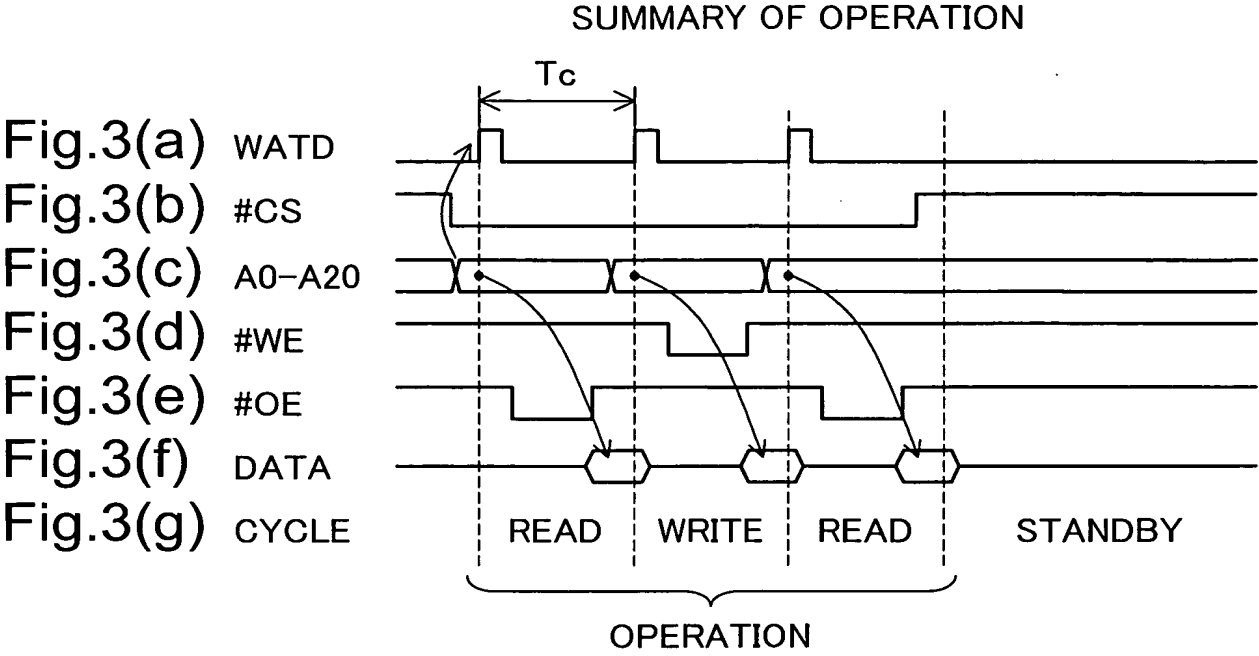


Fig.4

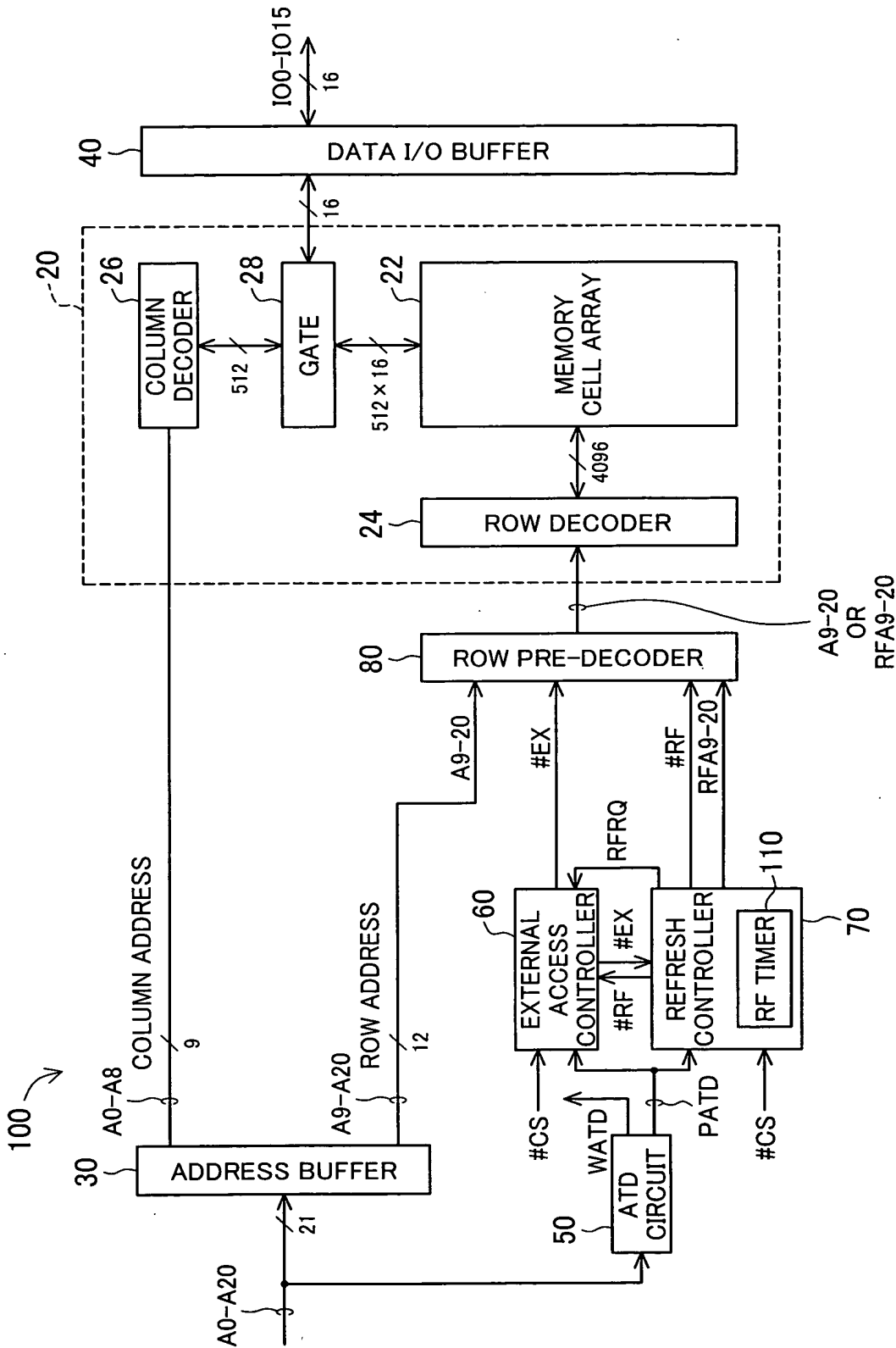


Fig.5

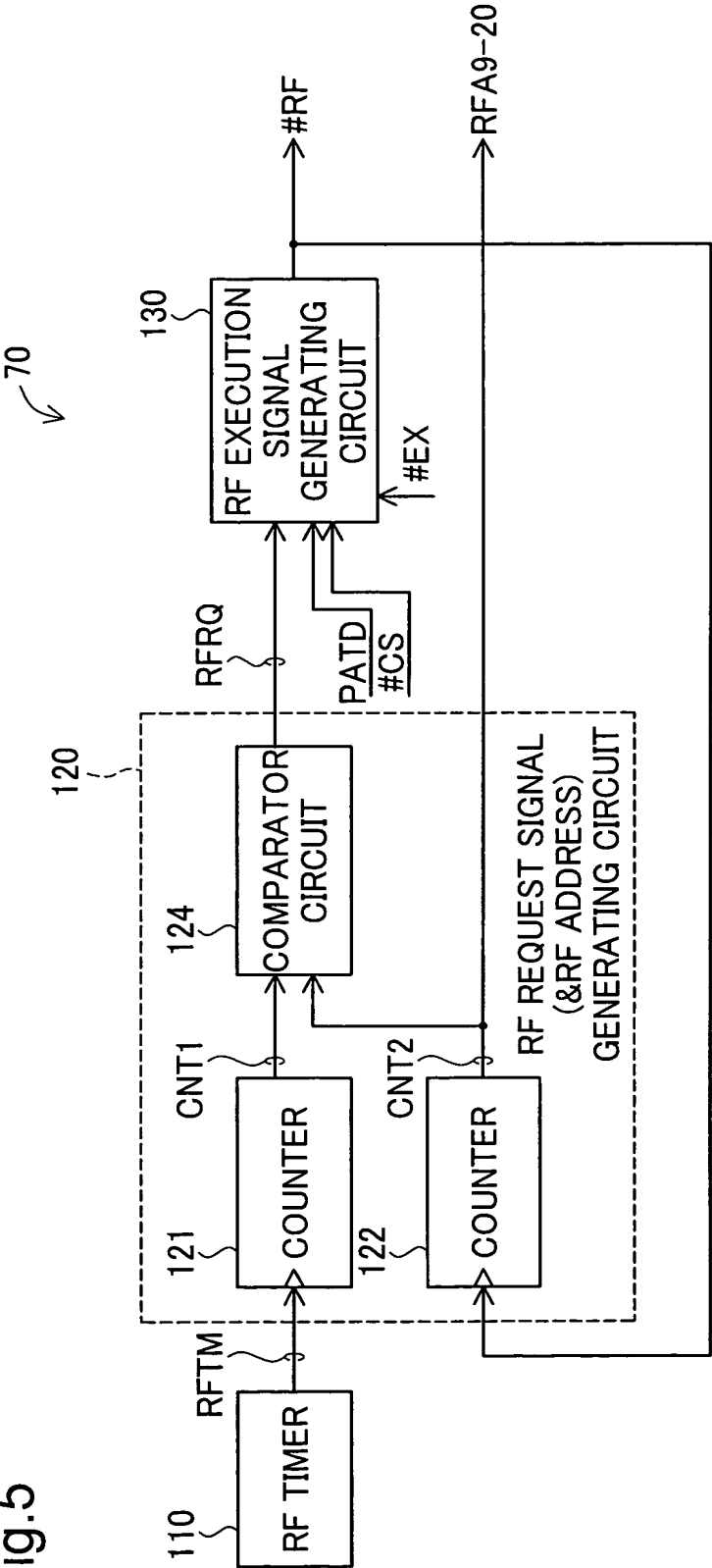
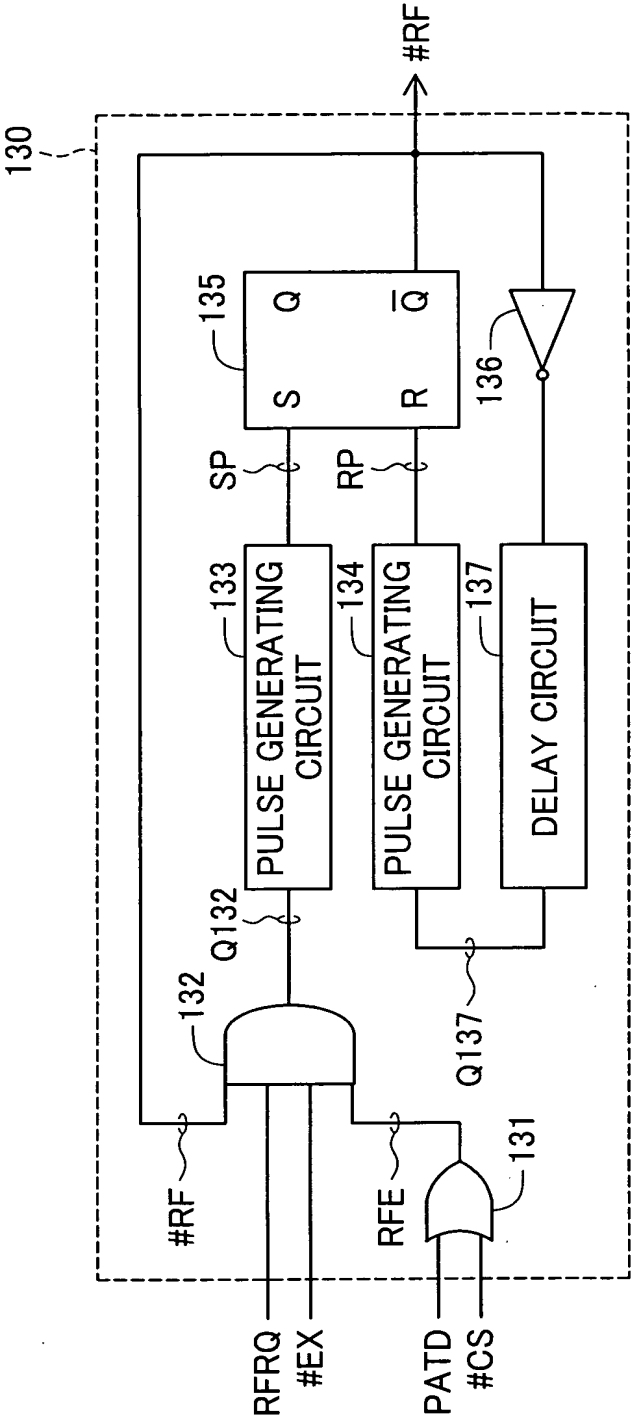


Fig.6



REFRESH OPERATION DURING OPERATION CYCLE

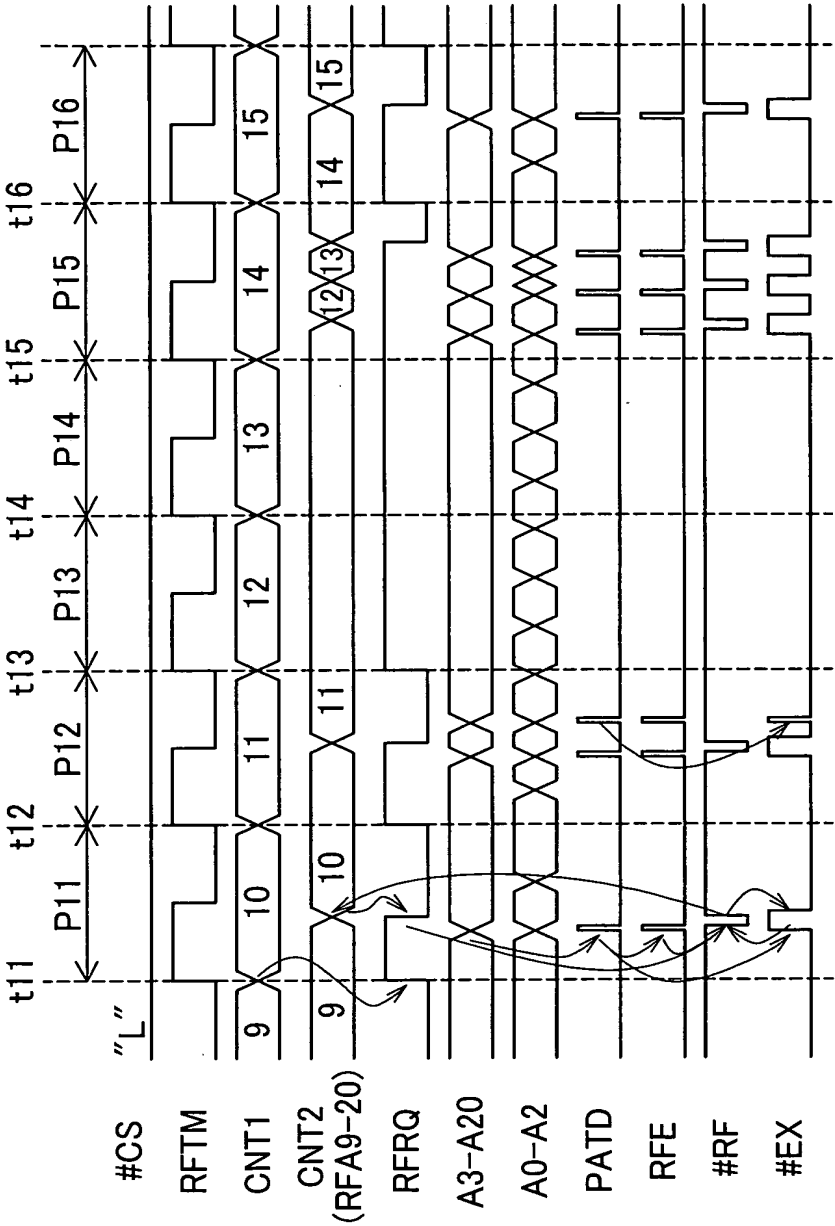
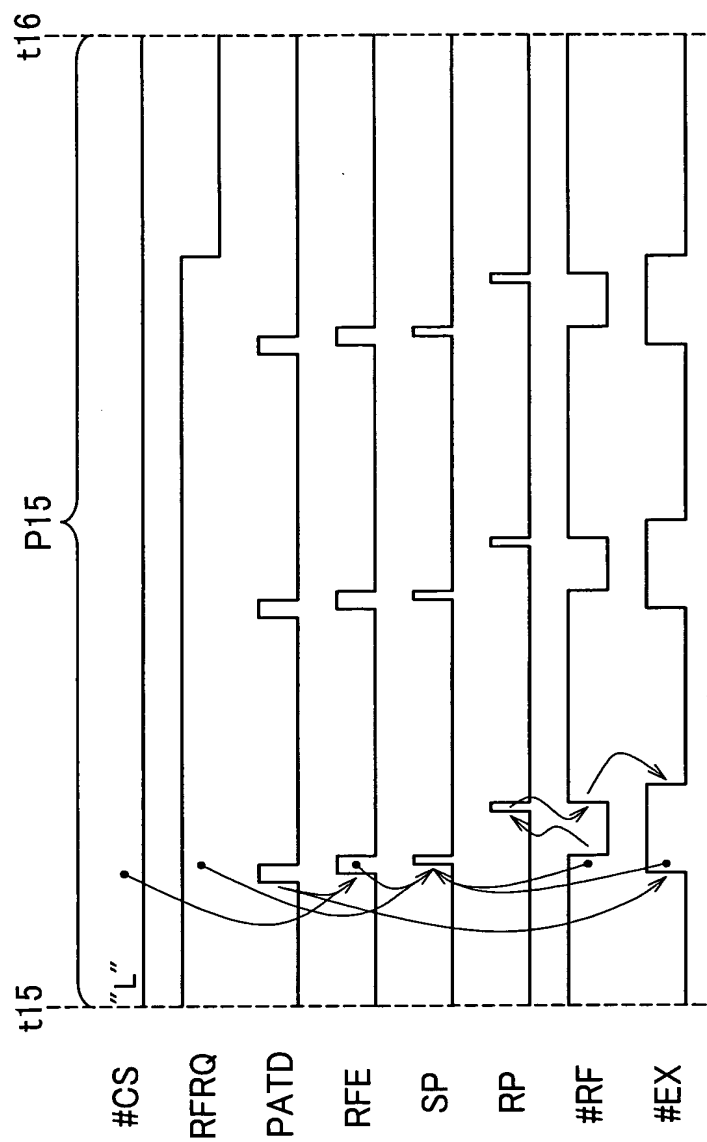


Fig.7(a)
Fig.7(b)
Fig.7(c)
Fig.7(d)
Fig.7(e)
Fig.7(f)
Fig.7(g)
Fig.7(h)
Fig.7(i)
Fig.7(j)
Fig.7(k)

Fig.8



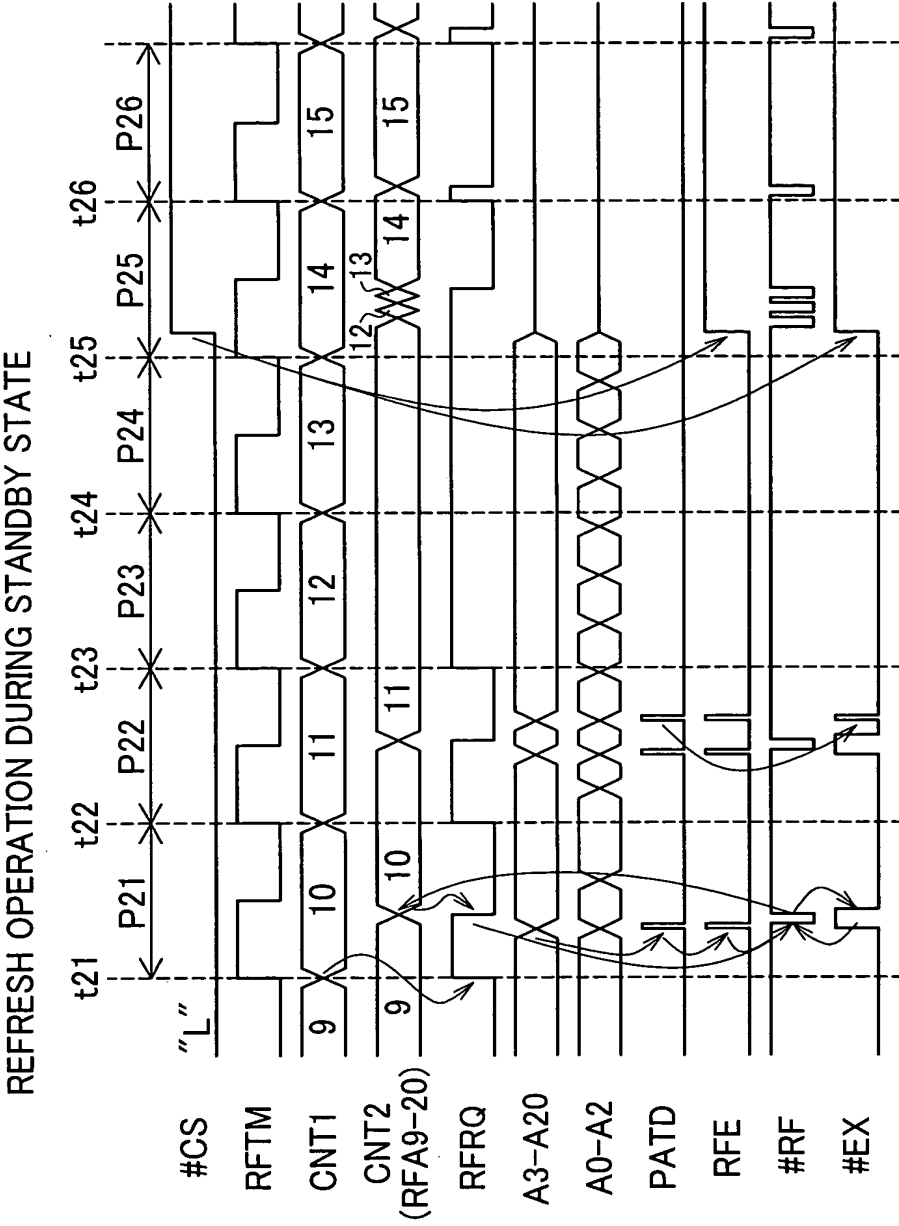


Fig.10

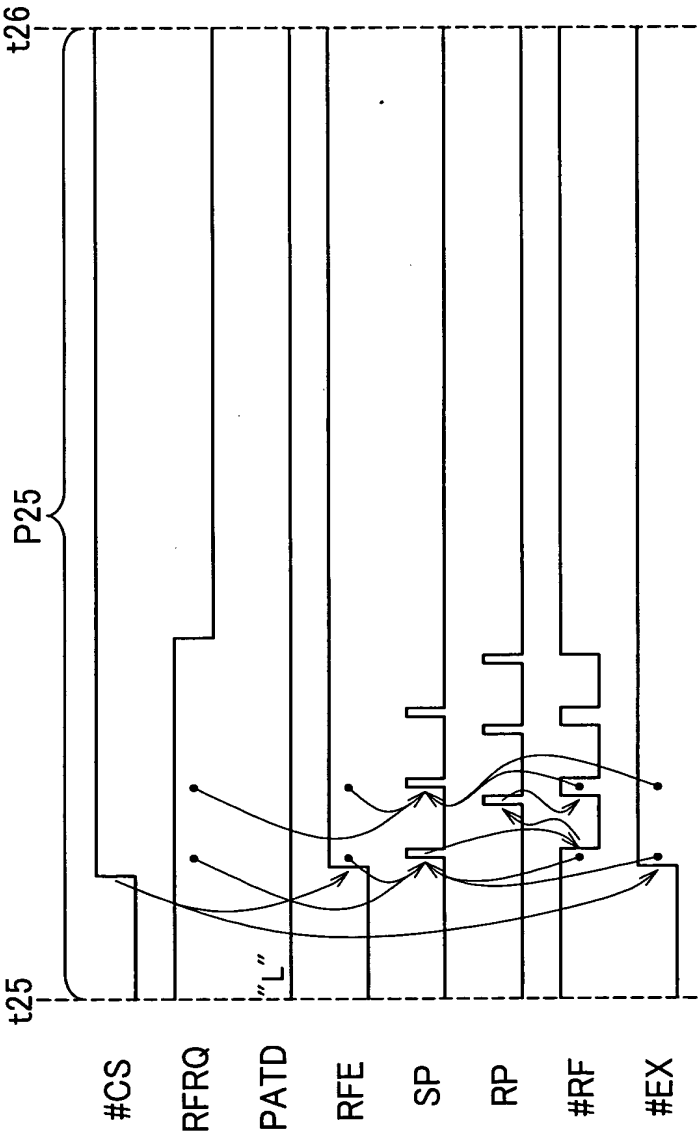


Fig.11

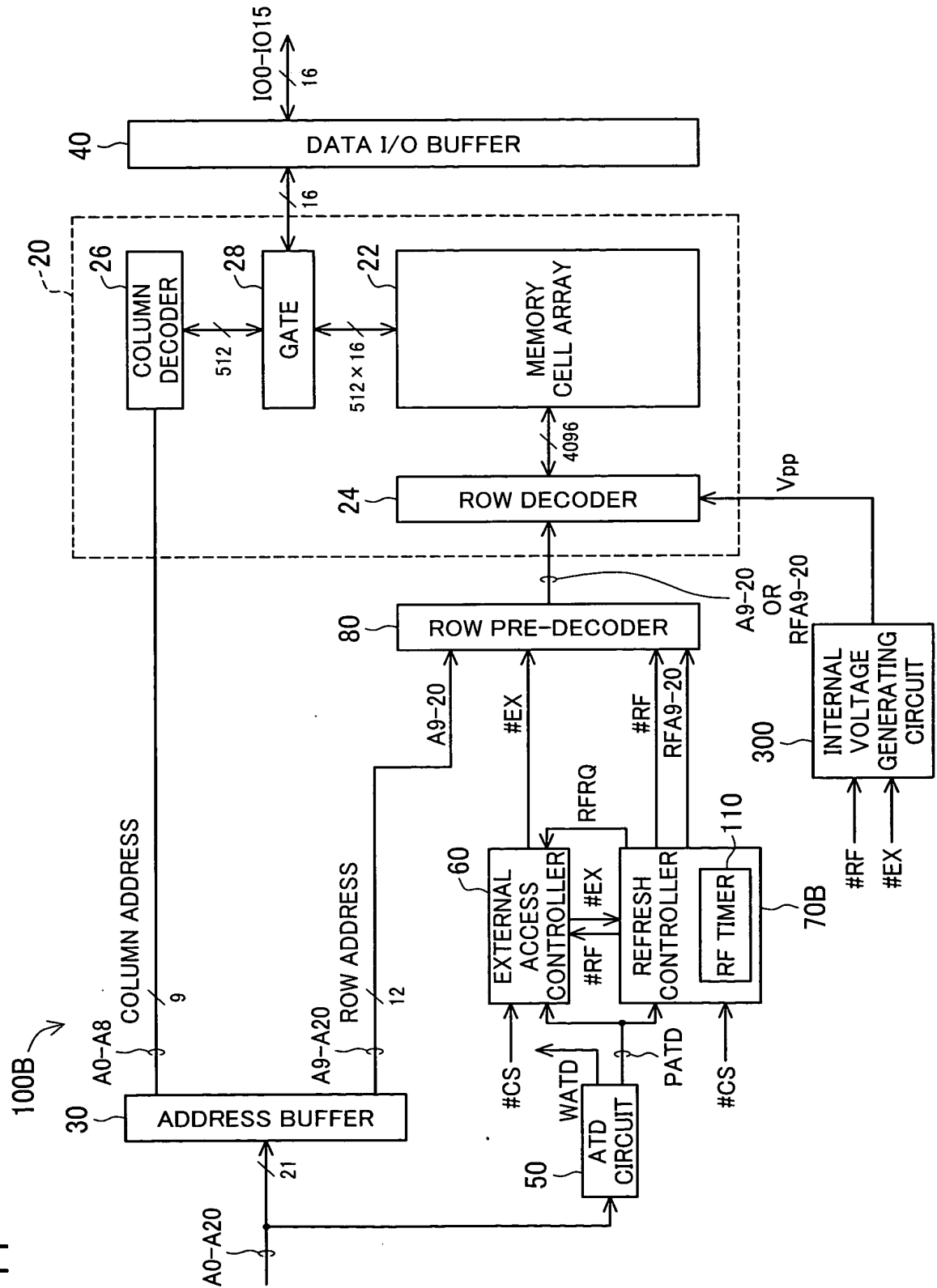


Fig.12

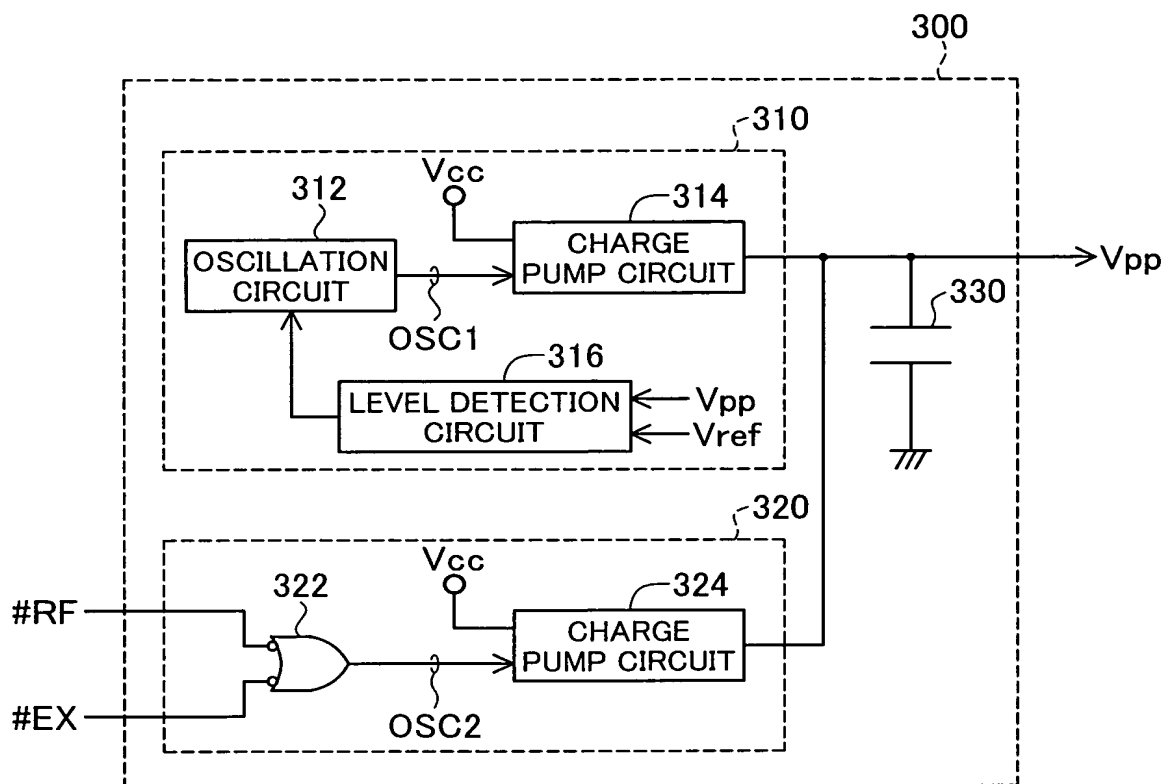


Fig.13

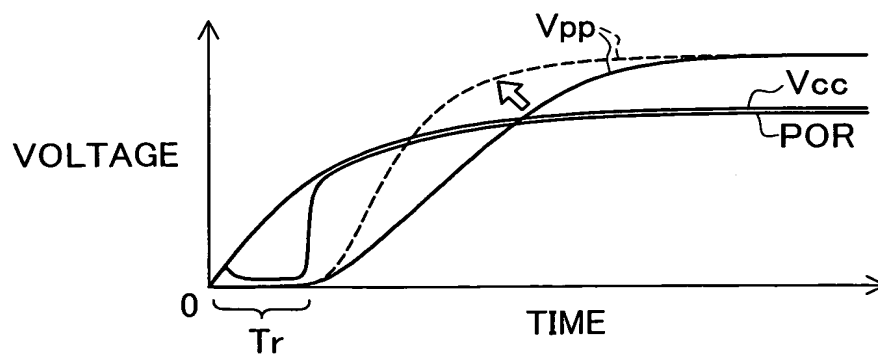


Fig.14

